SWITCHED-CAPACITOR RADIOFREQUENCY DELAY CIRCUITS FOR NEXT GENERATION WIRELESS SYSTEMS

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Abstract

In next generation communication systems, because of high frequency, massive MIMO with hundreds of antennas should be used to transmit sufficient power. This number of antennas naturally generates tens of nanoseconds of delay, which needs to be compensated later on. Whereas phase shifters only work for narrowband signals and digital delay circuits require analog circuits with harsh linearity, true time delay in the RF domain is useful. Since none of the previous RF delay circuit designs produce tens of nanosecond delay, a switched capacitor circuit with 144 paths is proposed and simulated in this thesis. The simulation result shows that around 10 ns delay was successfully generated for wideband signals. Moreover, the harmonic transfer function of a typical delay circuit from output to input is derived.

Subject Keywords: delay circuit; RF engineering; next generation communication; harmonic transfer functions; switched capacitor; linear periodic time variant

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1. Introduction

In next generation communication systems, carrier frequency is higher than in previous technologies. According to the Friis transmission equation (Eqn. 1), received power is proportional to $(\frac{N}{f_c})^2$, where N is the number of antennas, f_c is the carrier frequency, P_R and P_T are received power and transmitted power respectively, D and D_T are the corresponding antenna directivities, c is speed of light, and r is transmitting and receiving distance. It shows that in next generation communication, received power is significantly reduced if we keep the same number of antennas.

$$P_R = P_T D_T (\frac{c}{4\pi r})^2 D (\frac{N}{f_c})^2 \quad (1)$$

Because of this, the technique of massive multiple-input multiple-output (MIMO) is widely used. By using more antennas to transmit and receive signal, the beam power is more focused in one direction to improve coverage and avoid interference. By generating phase difference, one can steer the beam to the desired direction[1]. And by transmitting mutually orthogonal signals, one can communicate with multiple users simultaneously.

According to [2] and [3], massive MIMO with hundreds of antennas is recommended. Firstly, the capacity and spectral efficiency logarithmically increase with the number of antennas. Hundreds of antennas is a good balance between performance and cost. Secondly, energy efficiency is a quasi-concave function of the number of antennas in most cases. Hundreds of antennas is on the maximum point. If too many antennas are used, energy efficiency actually decreases.

Because of the potential travelling distance difference, significant delay can happen between different antennas. To make sure the signal is matched in the time domain when adding it up after receiving it from different antennas, one additional delay element in each path is needed to compensate for the natural delay difference. Previously, researchers mainly focused on phase shifters to mimic time delay because they are easier to implement and less bulky compared to true time delay elements. But phase shifters only work for narrowband signals because different frequencies in wideband signals experience different equivalent phase shifts when the same time delay is applied. In Figure 1, one should also see that the bandwidth of normalized gain when using phase shifters decreases significantly when we increase the number of antennas, which means phase shifters work even more poorly with wideband signals when we use massive MIMO technology [4]. Gain here is also known as array factor (AF). It is derived and discussed in more detail in Appendix A.

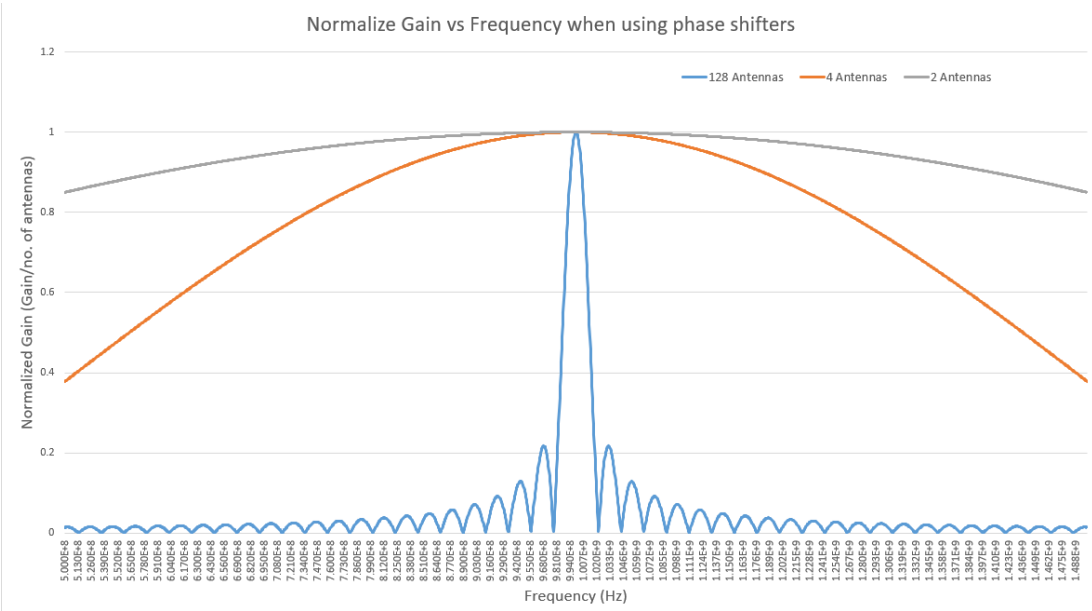

Figure 1: Gain / number of antennas (N) versus frequency when using phase shifters (plotted using Excel)[4] (Assume angle of incidence = 45 degrees, carrier frequency = 1 GHz and element spacing = half wavelength)

In addition, delay in digital domain is very cheap compared to delay in RF domain. But delay in the RF domain has its advantages. For example, [5] shows that by implementing delay in RF domain, we have analog spatial filtering to suppress interference. With less interference, the linearity requirement is less critical compared to delay in the digital domain. Thus, a design of a true time delay element is reasonable.

Engineers have designed true time delay elements based on transmission lines, filters or acoustic-based topologies [6]-[13]. But they only generate picosecond-scale delay, which is not sufficient in next generation massive MIMO systems. In Chapter 2.1, the delay needed is calculated. Chapter 2.2 simulates a single path circuit to get familiar with the idea. Chapter 2.3 illustrates method to increase delay. Chapter 2.4 simulates the designed 144-path circuit. Chapter 2.5 derives the harmonic transfer function of a typical delay circuit from input to output. Chapter 3 is a nice conclusion and suggestion for future research.

2. Description of Research Results

In this chapter, the maximum delay needed is calculated. A single path circuit is simulated. Then a corresponding multiple-path circuit is designed and simulated combining the two ideas above. Finally, a typical switched capacitor delay circuit is analyzed to find the harmonic transfer function from input to output.

2.1 Delay-needed calculation

For the true time delay element, the maximum delay required is $\frac{L}{c} sin\theta_{max}$, where L is array length, c is speed of light, and θ is angle of incidence. $L = (N-1)d$, where N is the number of antennas and d is antenna spacing. To make sure the waveform cancels out sideways, we design d as one half of the wavelength (λ), which is $\frac{1}{f_c}$, the carrier frequency. Finally, we substitute N = 100, f_c = 5 GHz in next generation communication systems, and θ_{max} = 45 degrees (Eqn. 2). It shows that we need a delay of 7 ns, which means that a delay of nanosecond scale, or even tens of nanoseconds is needed.

$$\tau_{max} = \frac{L}{c} sin\theta_{max} = \frac{(N-1)d}{c} sin\theta_{max} = \frac{(N-1)\lambda}{2c} sin\theta_{max} = (N-1)\frac{1}{2f_c} sin\theta_{max} \quad (2)$$

2.2 Single-path circuit simulation

To generate considerable delay, a switched-capacitor delay circuit design is proposed [14] (Figure 2). For simulation purposes, it is operated at a lower frequency: 100 kHz. It is composed of a capacitor (C_1) and two voltage-controlled switches connected to input signal and output

signal (S_1 & S_2) respectively. C_1 is designed such that its impedance is much larger compared to input impedance R, and voltage on C_1 is approximately the same as input voltage when S_1 is closed. When S_1 is closed and S_2 is open, C_1 reads the value of the input signal until S_1 opens again (Figure 3 pink path). Then S_2 closes to read from C_1 by output (Figure 3 red path). The switch closing time should be much larger than the time constant $\tau = RC$ such that the capacitor recharges or discharges sufficiently. By doing this process, delay is generated from input to output. But this topology has limitations on maximum achievable delay. To make sure that we recover the original signal from signal samples received in output, the sampling rate should be 2 times the maximum frequency of input signal (Nyquist rate). Because of this, C_1 has to release the old data to output and read a new value from input within the sampling period T.

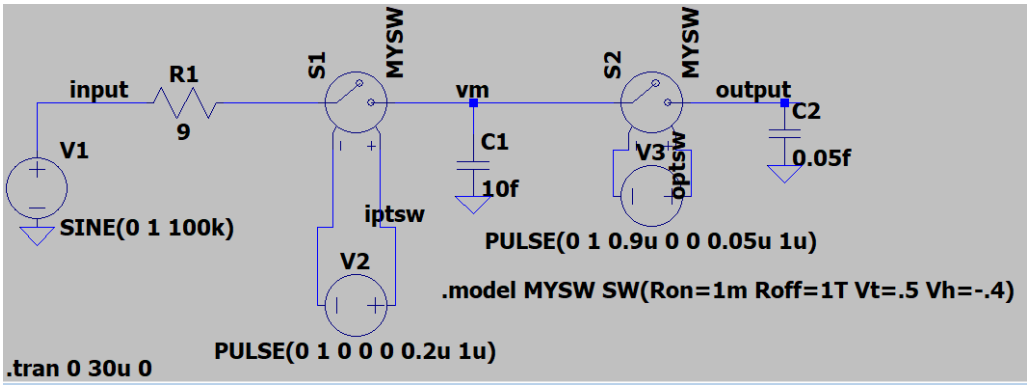

Figure 2: Single-path switched-capacitor delay circuit in low frequency (in LTSpice) [14]

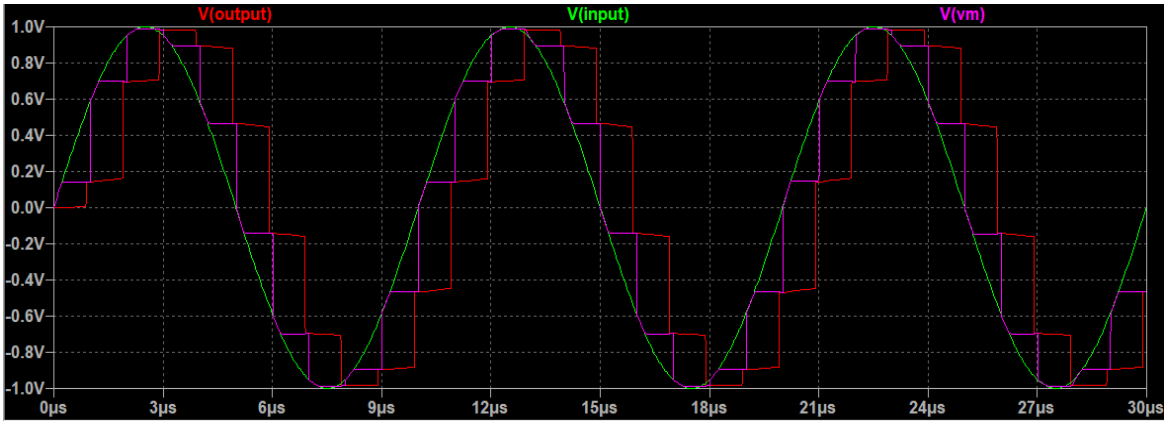

Figure 3: Single-path simulation with low frequency sinusoidal input (in LTSpice) [14]

2.3 Method to increase delay

To increase the maximum achievable delay, A multiple-path circuit is implemented(Figure 4). In this 4-path example, when the new sampling period reaches, instead of releasing the data to output and read the new value from input by path 1, path 2 stores the new data. Path 1 doesn't need to release and read until all of the other paths are occupied. Therefore, a N-path delay circuit roughly increases the maximum achievable delay by a factor of N.

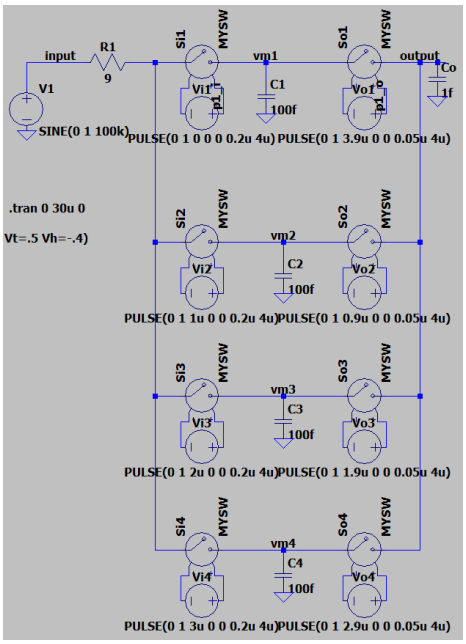

Figure 4: 4-path switched-capacitor delay circuit in low frequency (in LTSpice) [14]

2.4 144-path Delay Circuit Analysis and Simulation

Back in radio frequency, we generate a wideband RF signal by a sinc function multiplied by a carrier sinusoidal. Sinc function in time domain is a rectangular function in frequency domain (Eqn. 3). By increasing parameter a, the bandwidth of it increases accordingly. Then the carrier sinusoidal with radio frequency shifts it to RF domain. In the simulation below, a signal with carrier frequency 6 GHz, and bandwidth 1.2 GHz is used. The fractional bandwidth is $\frac{1.2\ GHz}{6\ GHz} =$

20% , which is considered a wideband signal (Eqn. 4). Since sinc is not causal and simulation always starts with t = 0, it is shifted in time by an appropriate amount, and magnitude plot in frequency should not be affected.

$$b \bullet sinc(a\pi t) \leftrightarrow \frac{b}{|a|} rect(\frac{f}{a}) \tag{3}$$

$$sinc(1.2 \times 10^9 \pi t) \cos(2\pi \times 6 \times 10^9 t) \tag{4}$$
$$\leftrightarrow \frac{1}{2.4 \times 10^9} rect\left(\frac{f - 6 \times 10^9}{1.2 \times 10^9}\right) + \frac{1}{2.4 \times 10^9} rect\left(\frac{f + 6 \times 10^9}{1.2 \times 10^9}\right)$$

The highest frequency of this signal is $6\ GHz + \frac{1.2\ GHz}{2} = 6.6\ GHz$. The minimum sampling frequency (Nyquist rate) is $6.6\ GHz \times 2 = 13.2\ GHz$, which corresponds to sampling period $T = \frac{1}{13.2\ GHz} = 0.075\ ns$. If 10 ns delay is needed, the delay circuit roughly has $\frac{10\ ns}{0.075\ ns} =$

134 $paths$. It is not harmful to use 144 paths (Figure 5), since the actual implemented delay is smaller than expected (the switches closing time needs to be much larger than time constant).

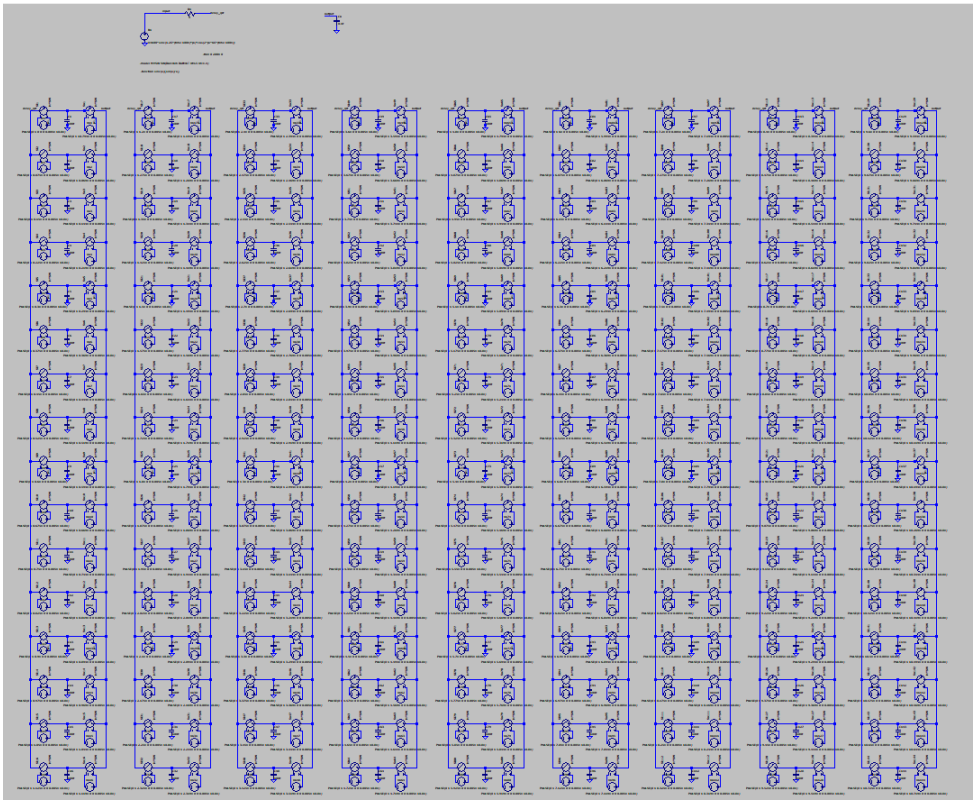

Figure 5: 144-path switched-capacitor delay circuit with RF wideband input (in LTSpice)

The simulation result is as expected. In time domain (Figure 6), the input is a sinc function modulated by a radio frequency cosine, shifted by 100 ns in purpose (green plot). The output (blue plot) is a delayed version of input by around 10 ns. In the frequency domain (Figure 7), the input is a wideband signal centered at 6 GHz with bandwidth 1.2 GHz (green plot). The output is a double-sided signal. The sampling frequency (6.6 GHz) is not the center frequency of input (6

GHz), so one of the sidebands comes from the positive part and the other comes from the negative one.

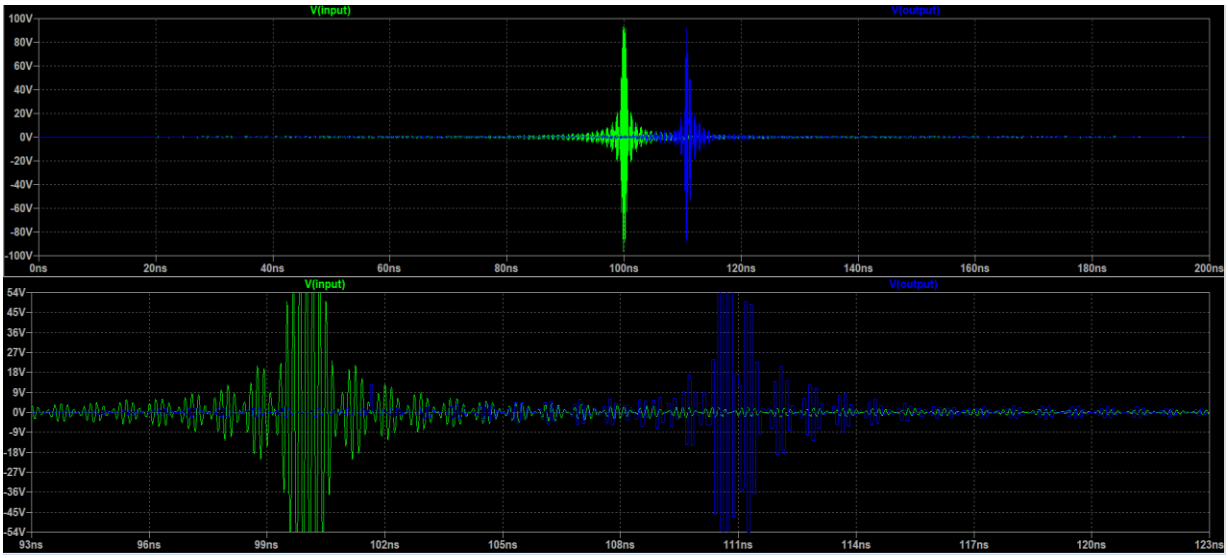

Figure 6: 144-path circuit simulation result in time domain (in LTSpice)

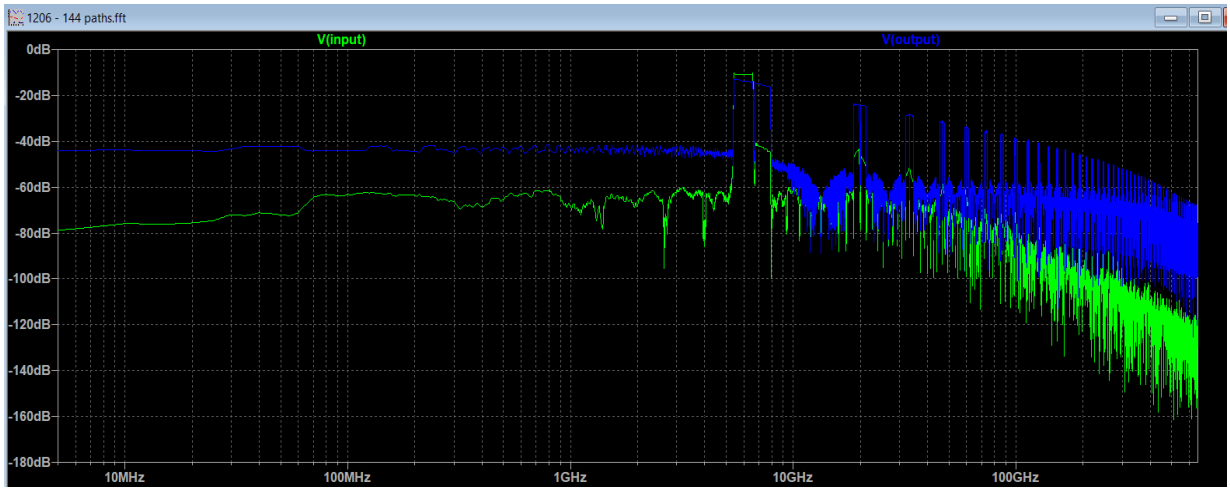

Figure 7: 144-path circuit simulation result in frequency domain (in LTSpice)

2.5 4-path Delay Circuit Analysis – Frequency Domain Output/Input Relationships

It is useful to derive the output and input relationship in frequency domain. For a linear time-invariant (LTI) system, input and output relationship is simply described by a transfer function (Fourier transform of the impulse response). Unfortunately, the switched capacitor delay circuit is not that simple: it is a linear time-variant system because of the existence of switches. Since the switches operates in a periodic way, it is considered as a linear periodic time-variant (LPTV) system, and its output $V_{out}(f) = \sum_{n=-\infty}^{\infty} H_n(f)V_{in}(f - nf_c)$, where $H_n(f)$ is called harmonic transfer function (in terms of n and f), f_c is the fundamental operating frequency of the system (frequency that it is periodic on), and $V_{in}(f)$ is the Fourier transform of the input signal. The main goal is to find HTF of the switched-capacitor delay circuit.

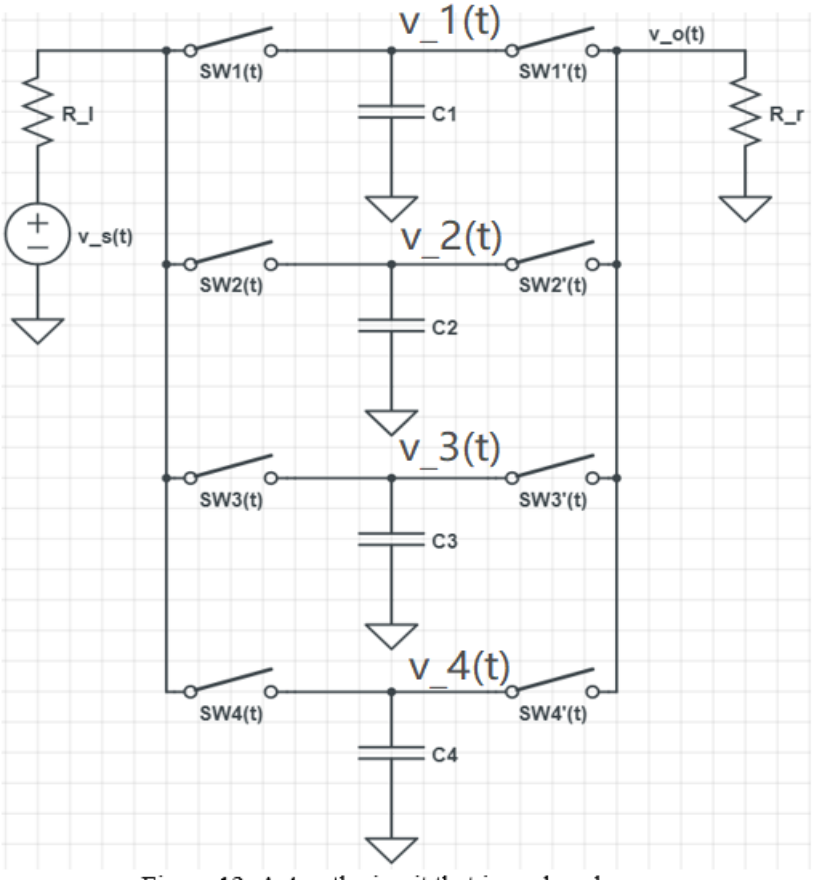

Figure 8: A 4-path circuit that is analyzed on

Consider a 4-path circuit as an example (Figure 8). $v_s(t)$ is the input signal. $v_o(t)$ is the output signal. $swk(t)$ is a periodic square wave that controls the switches such that it equals to 1 (switch on) when time t is in between $nT_c + (k-1)\tau$ and $nT_c + k\tau$, and 0 (switch off) else, where $T_c = \frac{1}{f_c}$ is the time period that the system is periodic on, $\frac{\tau}{T_c} = 25\%$ is the duty cycle of this specific 4-path circuit, k indicates a specific path, and n is an integer. $swk'(t) = swk(t - T_d)$, where T_d is such that $swk'(t)$ does not overlap with $swk(t)$. $C_k = C$. Let $v_{kr}(t) = v_k(t)swk'(t)$. Since it indicates the period when the right-side switch is on, it is also true that $v_{kr}(t) = v_o(t)swk'(t)$, which gives us Eqn. 5.

$$v_o(t) = \sum_{k=1}^{4} v_{kr}(t) \tag{5}$$

Notice that one path does not see each other, it is not harmful to only focus on the first path (k = 1) and temporarily erase the others (Figure 9). An exemplary analysis of a simpler one-port circuit was done in [15]. Based on their method, derivation for the two-port delay circuit is as following.

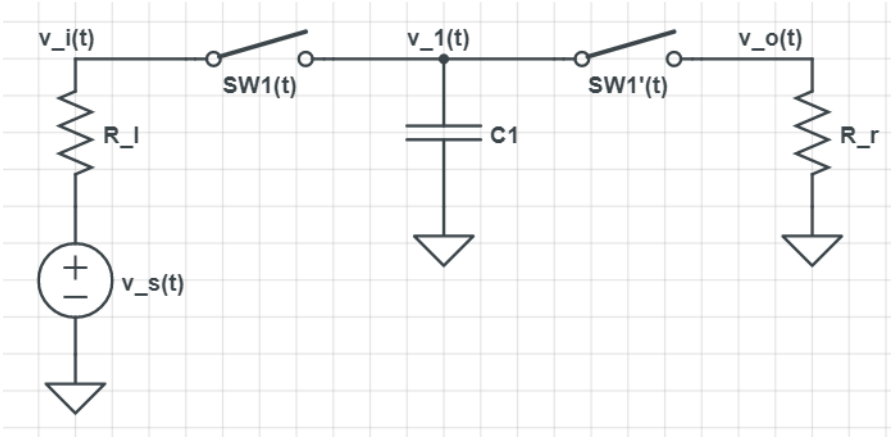

Figure 9: One-path circuit decomposed from Figure 8

When the right-side switch opens, $v_{1r}(t) = 0$. Thus, $\frac{d}{dt}v_{1r}(t) = 0$. When the right-side switch closes, it is described by a differential equation $\frac{d}{dt}v_{1r}(t) = -\frac{1}{R_rC}v_{1r}(t)$. At the instant switching moment, $v_{1r}(t)$ experiences an instant step of change from 0 to the value of $v_1(t)$ or the other way around, such that its time derivative should be a delta function. Based on the discussions above, a compact form of the time-domain relation is given as Eqn. 6.

$$\frac{d}{dt}v_{1r}(t) = -\frac{1}{R_rC}v_{1r}(t) + \sum_{n=-\infty}^{\infty} v_1(t)[\delta(t - T_d - nT_c) - \delta(t - T_d - nT_c - \tau)] \tag{6}$$

When the left-side switch closes, it satisfies the differential equation $\frac{d}{dt}v_1(t) = -\frac{1}{R_lC}v_1(t) + \frac{1}{R_lC}v_s(t)$. Solve for the equation with initial condition $v_1(t_0)$, where $t_0 = nT_c + (k-1)\tau = nT_c$ is the instantaneous left-side switch closing time (k = 1 for the first path), Eqn. 7 is obtained. Here we define $f_{rcl} = \frac{1}{2\pi R_lC}$ and $f_{rcr} = \frac{1}{2\pi R_rC}$.

$$v_1(t) = v_1(t_0)e^{-2\pi f_{rcl}(t-t_0)} + 2\pi f_{rcl}\int_{t_0}^{t} e^{-2\pi f_{rcl}(t-x)}v_s(x)dx \tag{7}$$

Note that Eqn. 7 is only valid within the closing period of the left-side switch. Assume that the input is sinusoidal: $v_s(t) = e^{j2\pi ft}$. Solve for the integral and plug in $t_0 = nT_c$ and $t = nT_c + \tau$, we get Eqn. 8, where $\beta = \frac{1}{1+j\frac{f}{f_{rcl}}}(e^{j2\pi f\tau} - e^{-2\pi f_{rcl}\tau})$.

$$v_1(nT_c + \tau) = v_1(nT_c)e^{-2\pi f_{rcl}\tau} + \beta e^{j2\pi fnT_c} \tag{8}$$

Using the same method for the right-half circuit, we get Eqn. 9 true for t within the closing period of the right-side switch, and $t_0 = nT_c + T_d$, instantaneous closing time of it. Plug in $t = nT_c + \tau + T_d$.

$$v_1(t) = v_1(t_0)e^{-2\pi f_{rcr}(t-t_0)} \tag{9}$$

$$v_1(nT_c + \tau + T_d) = v_1(nT_c + T_d)e^{-2\pi f_{rcr}\tau}$$

When no switch closes, $v_1(t)$ keeps its value. Thus, Eqn. 10 is true for all n.

$$v_1(nT_c + T_d) = v_1(nT_c + \tau) \tag{10}$$

$$v_1(nT_c + T_d + \tau) = v_1((n+1)T_c)$$

Combine Eqn. 10 with Eqn. 8 and 9, Eqn. 11 is obtained.

$$v_1((n+1)T_c + T_d) = v_1(nT_c + T_d)e^{-2\pi f_{rcr}\tau}e^{-2\pi f_{rcl}\tau} + \beta e^{j2\pi f(n+1)T_c} \tag{11}$$

Solve this difference equation using Z-transform.

$$v_1(nT_c + T_d) = G_p(f)e^{j2\pi f(nT_c+T_d)} \tag{12}$$

$$G_p(f) = \frac{\beta \cdot e^{j2\pi f(T_c-T_d)}}{e^{j2\pi fT_c} - e^{-2\pi(f_{rcl}+f_{rcr})\tau}} \tag{13}$$

Here, we come back to Eqn. 6 and generate Eqn. 14, Fourier transform of the impulse train. We replace back $e^{j2\pi ft} = v_s(t)$ because all signals could be viewed as superposition of sinusoidal signals. Equations above do not lose generality.

$$\sum_{n=-\infty}^{\infty} v_1(t)\delta(t - T_d - nT_c) = \sum_{n=-\infty}^{\infty} G_p(f)e^{j2\pi ft}\delta(t - T_d - nT_c) \tag{14}$$

$$= \sum_{n=-\infty}^{\infty} G_p(f)v_s(t)\delta(t - T_d - nT_c)$$

$$\overset{\mathrm{F}}{\leftrightarrow} \left[G_p(f)V_s(f)\right] * \sum_{n=-\infty}^{\infty} f_c\delta(f - nf_c)e^{-j2\pi nf_cT_d}$$

$$= \sum_{n=-\infty}^{\infty} G_p(f - nf_c)f_ce^{-j2\pi nf_cT_d}\,V_s(f - nf_c)$$

Similarly, from Eqn. 8, 9 and 10,

$$v_1\big((n+1)T_c + T_d + \tau\big) = e^{-2\pi f_{rcr}\tau}[v_1(nT_c + T_d + \tau)e^{-2\pi f_{rcl}\tau} + \beta e^{j2\pi f(n+1)T_c}] \tag{15}$$

$$v_1(nT_c + T_d + \tau) = G_n(f)e^{j2\pi f(nT_c+T_d+\tau)} \tag{16}$$

$$G_n(f) = G_p(f)e^{-j2\pi f\tau}e^{-2\pi f_{rcr}\tau} = \frac{\beta \cdot e^{j2\pi f(T_c-T_d)}}{e^{j2\pi fT_c} - e^{-2\pi(f_{rcl}+f_{rcr})\tau}}e^{-j2\pi f\tau}e^{-2\pi f_{rcr}\tau} \tag{17}$$

Analogous to Eqn. 14, we obtain the Fourier transform for the other impulse train.

$$\sum_{n=-\infty}^{\infty} v_1(t)\delta(t - T_d - nT_c - \tau) = \sum_{n=-\infty}^{\infty} G_n(f)e^{j2\pi ft}\delta(t - T_d - nT_c - \tau) \tag{18}$$

$$= \sum_{n=-\infty}^{\infty} G_n(f)v_s(t)\delta(t - T_d - nT_c - \tau)$$

$$\overset{\mathrm{F}}{\leftrightarrow} [G_n(f)V_s(f)] * \sum_{n=-\infty}^{\infty} f_c\delta(f - nf_c)e^{-j2\pi nf_c(T_d+\tau)}$$

$$= \sum_{n=-\infty}^{\infty} G_n(f - nf_c)f_c e^{-j2\pi nf_c(T_d+\tau)} V_s(f - nf_c)$$

Finally, we do Fourier transform of entire Eqn. 6 and get Eqn. 19.

$$V_{1r}(f) = \sum_{n=-\infty}^{\infty} H_{1n}(f)V_s(f - nf_c) \tag{19}$$

$H_{1n}(f)$ is the harmonic transfer function (HTF) from $V_s(f)$ to $V_{1r}(f)$, and it is given in Eqn. 20.

$$H_{1n}(f) = \frac{1}{j2\pi f + 2\pi f_{rcr}}[G_p(f - nf_c)f_c e^{-j2\pi nf_c T_d} - G_n(f - nf_c)f_c e^{-j2\pi nf_c(T_d+\tau)}] \tag{20}$$

For the k-th path, we define $t' = t - (k-1)\tau$ and find out $swk(t) = sw1(t - (k-1)\tau) = sw1(t')$ and $swk'(t) = sw1'(t')$, similarly. We define $v'_{kr}(t') = v_{kr}(t' + (k-1)\tau) = v_{kr}(t)$, and $v'_s(t') = v_s(t' + (k-1)\tau) = v_s(t)$. Here, the newly defined $v'_{kr}(t')$ and $v'_s(t')$ with time variable t' are on a circuit with controlling signals $sw1(t')$ and $sw1'(t')$. This condition is exactly the same as the 1st-path derivation above. Hence, Eqn. 21 is realized.

$$V_{kr}'(f) = \sum_{n=-\infty}^{\infty} H_{1n}(f)V_s'(f - nf_c) \tag{21}$$

Apply properties of Fourier transform:

$$V_{kr}(f)e^{j2\pi f(k-1)\tau} = \sum_{n=-\infty}^{\infty} H_{1n}(f)V_s(f-nf_c)\, e^{j2\pi(f-nf_c)(k-1)\tau} \tag{22}$$

$$V_{kr}(f) = \sum_{n=-\infty}^{\infty} H_{1n}(f)e^{-j2\pi nf_c(k-1)\tau}V_s(f-nf_c)$$

Combined with Eqn. 5 and 22 we find

$$V_o(f) = \sum_{n=-\infty}^{\infty}\sum_{k=1}^{4} e^{-j2\pi nf_c(k-1)\tau}H_{1n}(f)\, V_s(f-nf_c) \tag{23}$$

Hence, HTF of the entire circuit is given as

$$H_n(f) = \sum_{k=1}^{4} e^{-j2\pi nf_c(k-1)\tau}H_{1n}(f) \tag{24}$$

To test this result, consider a 4-path circuit in Figure 10. The input is a sinusoidal signal with a certain frequency. The switches operate with period $T_c = \frac{1}{f_c} = 1\ ns$. The switch closing time $\tau = \frac{1}{4}T_c = 0.25\ ns$ such that the duty cycle is ¼. Delay between left and right-side switch $T_d = 0.5\ ns$. $R_r = R_l = 50\ \Omega$ and $C = 100$ pF. In this circuit, duty cycle of switches is reduced a little bit so that no unwanted overlaps are identified by the simulator. Several input frequencies were simulated at, and the results are shown in Table 1, recording gain magnitude from output to input at this frequency.

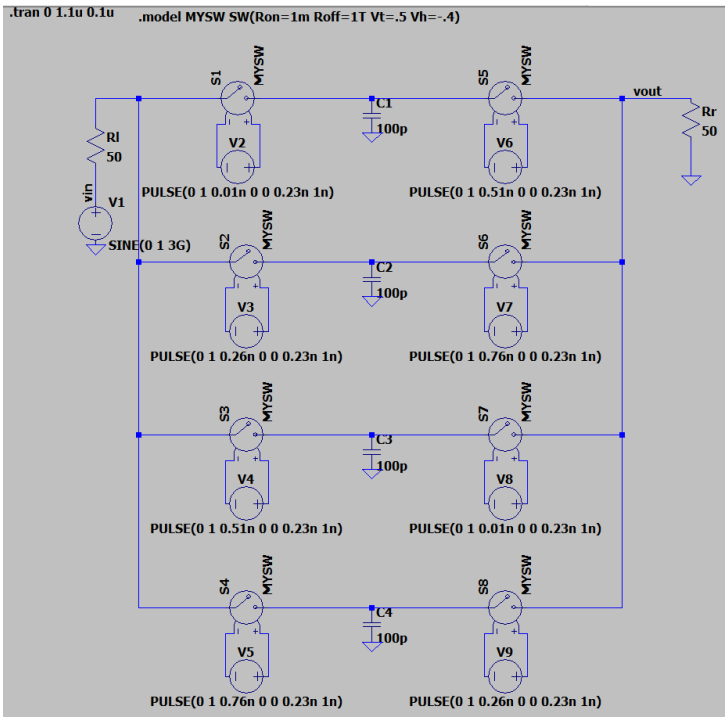

Figure 10: 4-path circuit simulated by LTSpice

Table 1: 4-path circuit simulation result and comparison with |HTF| at n = 0

Input harmonic frequency (GHz)	|Vin(f)| at this frequency	|Vout(f)| at this frequency	|Vout(f)/Vin(f)| at this frequency	|Vout(f)/Vin(f)| at this frequency (20 dB)	$\lvert H_0(f)\rvert$ at this frequency (20 dB)
0.2	707.1	29.6	0.0419	-27.56	-27.49

0.5	706.5	16.7	0.0236	-32.5	-32.5
1	704.4	285.29	0.405	-7.85	-7.883
2	703.2	271.94	0.387	-8.25	-13.93
2.4	703.3	4.7	6.683E-3	-43.5	-43.56
3	702.9	31.6	0.04496	-26.94	-27
4.5	701.2	0.186	2.653E-4	-71.53	-70.55

Most gain magnitudes matched pretty well with HTF magnitudes (|HTF|) at n = 0 (fundamental transfer function). This is because in most single-tone cases, only HTF at n = 0 multiplied with input at input frequency contributes to the output at input frequency. Except for input frequencies at integer multiples of switching frequency, where the corresponding negative frequency multiplied with HTF at n > 0 might not be negligible. In this case, when the input frequency is 2 GHz, HTF at n = 4 multiplied with negative frequency part of input deviates the gain from |HTF| at n = 0 when added with the contribution of positive frequency part in complex domain.

In Figure 11, a continuous plot of |HTF| at n = 0 with dot-marked magnitude gain from simulation results is shown.

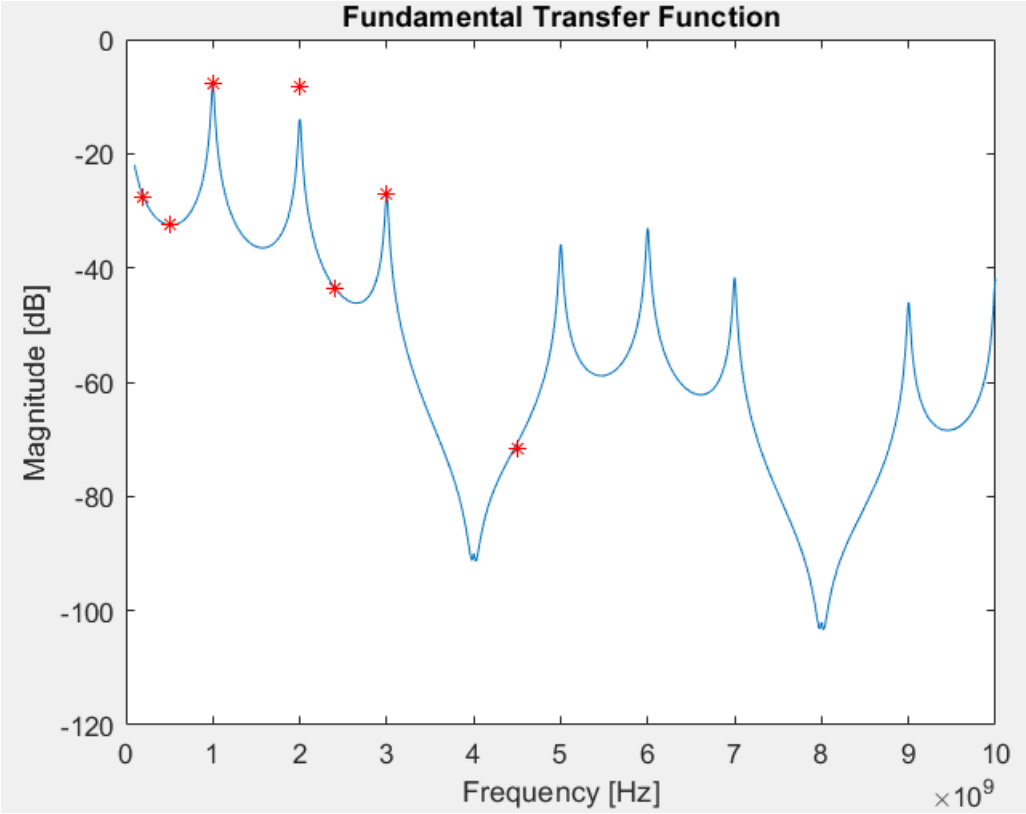

Figure 11: plot of |HTF| at n = 0 (blue ink) with dot-marked magnitude gain from simulation results (red dots) in MATLAB

3. Conclusion

The massive MIMO concept is useful in high speed next generation communication systems. Because of the delay nature of massive MIMO antennas, a true-time RF delay circuit is useful for compensation, with low linearity requirement and higher bandwidth. Whereas previous topologies failed to construct sufficient delay, switched capacitor delay circuits do this job easily by constructing multiple paths. Around 10 ns delay is available with 144-path delay circuit and it is clearly simulated in this thesis. A useful derivation of input and output relationships of a typical delay circuit in frequency domain is given. The delay circuit designed and analyzed in this thesis sufficiently compensates natural delay in massive MIMO systems for wideband signals. In the future, more research could be done to make the circuit less bulky.

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Appendix A Array Factor Derivation and Plot

In Figure 1, a plot of normalized gain versus frequency with different numbers of antennas (N) using phase shifters is given. Phase shifters give us constant phase change, which mimics different amount of time delay for different frequencies. But the natural delay is the same for all frequencies. For wideband signals, phase shifters are designed such that they work perfectly at carrier frequency. For other frequencies of the signal, the phase-mimicked time delay does not match with the amount of natural delay, and the outputs of phase shifters of different path are out of phase. When out-of-phase signals add up, they cancel out to some extent. Using knowledge of phasors, we add up sinusoidal signal output from all paths at different frequencies, and plot the magnitude of the summed output divided by N (normalized gain or normalized array factor) versus frequency. This is how Figure 1 was plotted using Microsoft Excel. In this chapter, an alternative way of obtaining the plot in Figure 1 is given, by directly deriving the expression of array factor.

Suppose we have a N-element 1D antenna array with serial number i = 1 to i = N. They experience a natural delay of $\Delta\tau = \frac{d}{v}sin\theta$, where d is the antenna element spacing, v is the wave velocity, and θ is the angle of incidence. For each antenna element, a subsequent delay element generates a delay of $\tau_i = (N - i + 1)\tau_s$, where τ_s is the delay step between consecutive elements. Suppose N = 2M (M integer) is even, and the incidence wave is a sinusoidal signal $s(t) = Acos(\omega t)$. After the signal passing through the delay element and experienced the corresponding two delays above, signal received for each element becomes Eqn. 25.

$$s_{i,d}(t) = Acos(\omega(t - (i-1)\Delta\tau - \tau_i)) \tag{25}$$

After summing up the signal, it becomes Eqn. 26.

$$s_{sum}(t) = A\sum_{i=1}^{2M}\cos\left(\omega(t-(i-1)\Delta\tau-(2M-i+1)\tau_s)\right) \tag{26}$$

$$\frac{s_{sum}(t)}{A} = \cos\big(\omega(t-2M\tau_s)\big) + \cos\big(\omega(t-\Delta\tau-(2M-1)\tau_s)\big) + \cdots$$

$$\ldots + \cos\big(\omega(t-(2M-2)\Delta\tau-2\tau_s)\big) + \cos\left(\omega(t-(2M-1)\Delta\tau-\tau_s)\right)$$

Using trig identities, Eqn. 27 is obtained.

$$\frac{s_{sum}(t)}{2A} = \cos\left(\frac{1}{2}\omega(2t-(2M-1)\Delta\tau-(2M+1)\tau_s)\right)\times \tag{27}$$

$$\left[\cos\left(\frac{1}{2}\omega((2M-1)\Delta\tau-(2M-1)\tau_s)\right) + \cos\left(\frac{1}{2}\omega((2M-3)\Delta\tau-(2M-3)\tau_s)\right) + \cdots\right.$$

$$\left.\ldots + \cos\left(\frac{1}{2}\omega(\Delta\tau-\tau_s)\right)\right]$$

$$= \cos\left(\frac{1}{2}\omega(2t-(2M-1)\Delta\tau-(2M+1)\tau_s)\right)\sum_{k=1}^{M}\cos\left(\frac{1}{2}\omega(\Delta\tau-\tau_s)(2k-1)\right)$$

To simplify the summation, note that $\cos(\varphi(2k-1)) = Re\{e^{j\varphi(2k-1)}\}$, where $\varphi = \frac{1}{2}\omega(\Delta\tau-\tau_s)$. Thus,

$$\sum_{k=1}^{M}\cos(\varphi(2k-1)) = Re\{\sum_{k=1}^{M} e^{j\varphi(2k-1)}\} = Re\{\frac{e^{j\varphi(2M+1)} - e^{j\varphi}}{e^{j\varphi 2} - 1}\} \tag{28}$$

$$= Re\left\{e^{j\varphi}\frac{e^{j\varphi M}(e^{j\varphi M} - e^{-j\varphi M})}{e^{j\varphi}(e^{j\varphi} - e^{-j\varphi})}\right\} = \frac{\sin(\varphi M)}{\sin(\varphi)}\cos(\varphi M) = \frac{\sin(\varphi N)}{2\sin(\varphi)}$$

Finally, array factor (AF) is given as Eqn. 29. Ideally, we design $\tau_s = \Delta\tau$ such that AF reaches its maximum value at N. AF divided by number of antennas N gives us normalized gain.

$$AF = \frac{\sin(\frac{N}{2}\omega(\Delta\tau - \tau_s))}{\sin(\frac{1}{2}\omega(\Delta\tau - \tau_s))} \tag{29}$$

For phase shifters, we design the amount of phase shift $\rho_f = \frac{\Delta\tau}{2\pi f_c}$, where f_c is the carrier frequency of the signal. Thus, $\tau_s = 2\pi f\rho_f = \frac{f\Delta\tau}{f_c}$. Specifically for the example in Figure 1, we choose carrier frequency $f_c = 1\ GHz$, angle of incidence θ = 45 degrees and antenna spacing d is half wavelength of carrier frequency. A plot of normalized AF versus frequency for different numbers of antennas (N) is given in Figure 12. It is indeed same as Figure 1. Note that the -3 dB beamwidth is approximately $\frac{2}{N-1}$ for half-wavelength-spacing arrays. It shows that for massive

MIMO systems with large N, the bandwidth is indeed very small when using phase shifters. So it does not apply to wideband signals.

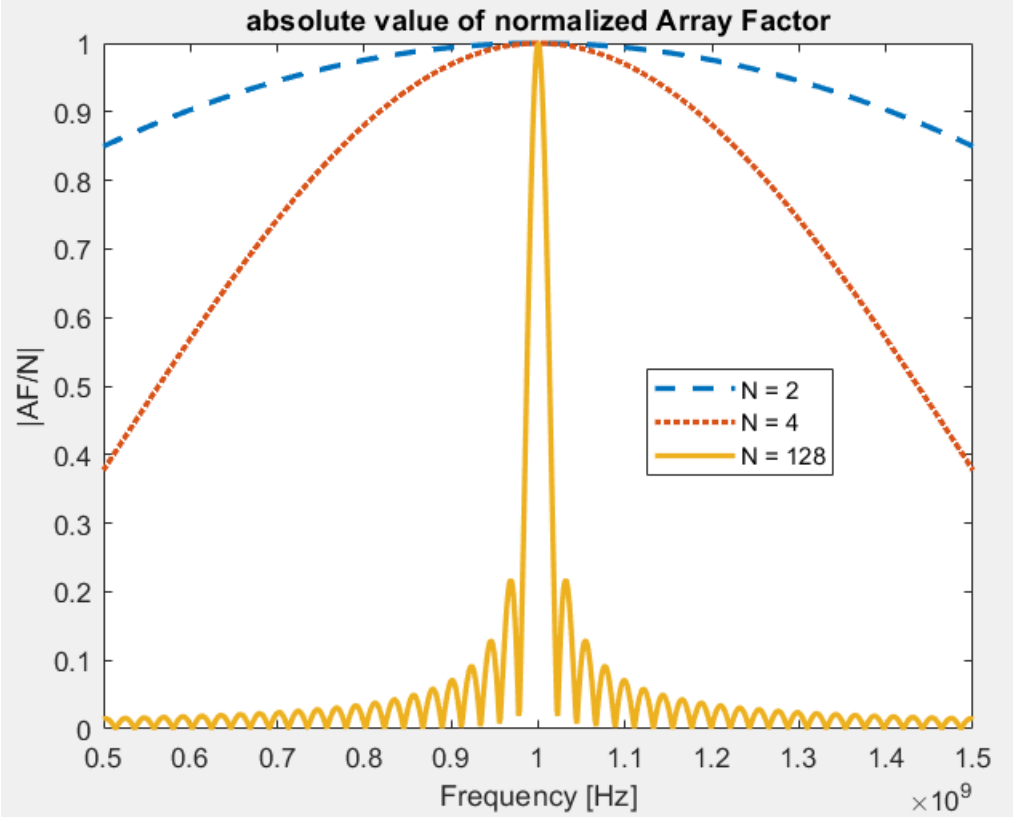

Figure 12: plot of |AF/N| versus frequency for the example in Figure 1 in MATLAB